COMPATIBLE CURRENT SINKING LOGIC

by Abe Marder and Ralph Bennett

INTRODUCTION

What Is Compatible Logic?

Fairchild classified all digital integrated circuits into compatible logic groups: current sinking logic, current sourcing logic, and current mode logic. A current sinking logic gate (for example, a DTL gate) draws current into its output ("sinks" current) when in a low state, and draws virtually no current when in the high state. A current sourcing gate (for example, an RTL gate) drives current out of its output in the high state, and except for minor leakage, drives no current in the low state. Current mode logic can draw or drive current in both states.

Compatible Current Sinking Logic

There are three families within the Fairchild current sinking group: TTμL (Transistor-Transistor Micrologic®), DTμL (Diode-Transistor Micrologic®), and LPDTμL (Low-Power Diode Transistor Micrologic®) integrated circuits. By crossing traditionally distinct family boundaries within this compatible logic group, you can optimize your system design.

With CCSL, the design engineer is freed from trade-off, in that he can take advantage of the speed of TTμL and the very low power requirements of LPDTμL in the same system. As a result, he is free to think in terms of what his applications need at each stage and not in terms of what one family can offer or what he will have to accept.

The engineer need no longer think in terms of logic families, such as DTμL and TTμL, but in terms of what his system needs at each particular stage. In other words, he can now design his ideal system, knowing that he can find the circuits with which to build it, and that their strict family identity is of no consequence. He doesn't have to study a logic family first and then decide what it will let him build. This new freedom offers the designer several unique advantages:

(1) He does not have to compromise, but can build the state-of-the-art system he really wants.
(2) He has a much wider range of choice. CCSL increases his design prerogative by providing him with the flexibility to design a truly unique system.
(3) He gains the advantage of maximum efficiency at minimum cost.

Finally, attention should be given to the new complex functions that will be an extension of the CCSL concept, designed for flexibility and for compatibility with existing functions. CCSL clears the way for the future by establishing a strong base, compatible within itself, for the complex functions. Functions such as four-bit shift registers with parallel input/serial output, as well as serial input/parallel output; and dual one-bit full adders which may be used as parity checkers. Were these functions to be restricted to use within one specific family, the design engineer would be needlessly handicapped. As an integral part of CCSL, they will enable him to realize state-of-the-art systems at minimum cost.

In order to realize the CCSL concept, a set of normalized rules for intermixing the three families had to be generated. These new loading rules are shown in detail in the following section of this Application Bulletin. The last section contains some typical applications with explanations which show how these systems are optimized using CCSL elements and applying the loading rules explained in the next section.

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LOADING RULES

The first step towards realization of a compatible logic family is to establish optimized input-output logic levels. These levels determine the noise immunity for all the elements, as well as the basis for system interfacing.

Fairchild CCSL loading rules guarantee the optimum logic levels over the full military temperature range of -55°C to ±125°C with V_{CC} supply within the range of 5V ±0.5V. These same logic levels, as well as the input load and output drive factors are also guaranteed over the temperature range of -20°C to ±100°C, for all CCSL elements. These guaranteed levels are:

Low-level output voltage (V_{OL}) = 0.4V
High-level output voltage (V_{OH}) = 2.5V
Low-level input voltage (V_{IL}) = 0.7V
High-level input voltage (V_{IH}) = 2.1V

Noise immunity is derived from the above numbers according to the following equations.

High-level noise immunity = $V_{OH} - V_{IH}$
Low-level noise immunity = $V_{IL} - V_{OL}$

Once the logic levels and dc noise margins are established, interfacing rules can be resolved. To simplify input loading and output drive capability, load factors and drive factors were assigned to each element. These factors are written as a ratio, but are not defined as an arithmetic ratio. The numerator can be added or subtracted independent of the denominator and vice versa. This ratio form was chosen for ease of interfacing analysis.

$$\text{Load Factor} = \frac{\text{High-level load factor}}{\text{Low-level load factor}} \left(\begin{matrix}\text{Shown as ratio on} \\ \text{inputs to circuits}\end{matrix}\right)$$

$$\text{Drive Factor} = \frac{\text{High-level drive factor}}{\text{Low-level drive factor}} \left(\begin{matrix}\text{Shown as ratio on} \\ \text{inputs to circuits}\end{matrix}\right)$$

where:

High-level load factor ≡ Input current drawn <u>into</u> the inputs, during the high-input level state.

Low-level load factor ≡ Input current drawn <u>out of</u> the input during the low-input level state.

High-level drive factor ≡ Ability of the output to supply current <u>out of</u> the output during the high-output level state.

Low-level drive factor ≡ Ability of the output to sink current <u>into</u> the output during the low-output level state.

A necessary condition is that the high-level drive factor must be equal to or greater than the sum of the driven high-level load factors <u>and</u> the low-level drive factor must be equal to or greater than the sum of the driven low-level load factors. Both high-level drive and load factors and low-level drive and load factors must be considered if efficient interfacing is to be accomplished.

The load factors given are based on worst case conditions at both V_{CC} 4.5 at -55°C and at +125°C. Input low-level load factors are guaranteed with the low-level output voltage (V_{OL}) applied to the inputs, which high-level load factors are tested with arbitrarily selected voltages much higher than the V_{OH} value.

If the temperature range is restricted to -40°C to +100°C or the V_{CC} range to 4.75 to 5.25 volts, a 10 percent increase in drive factors may be used.

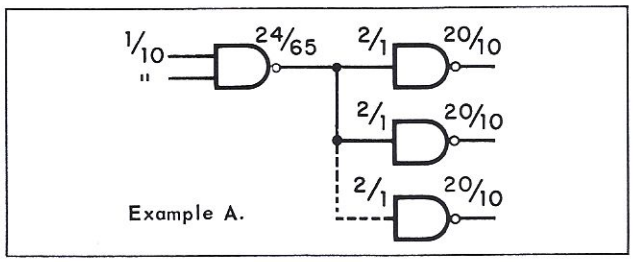


Fig. 1. DTμL Gate (6-K pullup) driving LPDTμL Gates.

$$\frac{24}{65} \geq \frac{2 + 2 + \cdots + 2}{1 + 1 + \cdots + 1}$$

Maximum load = 12 LPDTμL gates. Limited by the high-level drive capabilities. In this case, the low-level load is only 12, and the drive capability is 65. Reference to the curves shown in Fig. 3, will show this node to have a maximum V_{OL} = 100mV and therefore a worst case low level noise immunity of 0.6 volts.

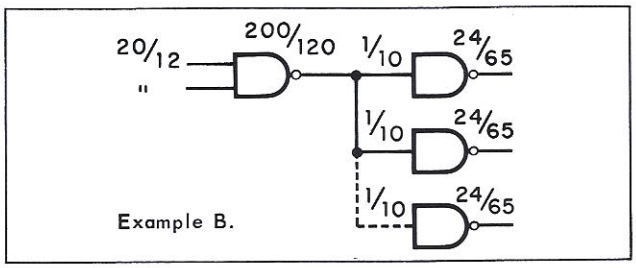


Fig. 2. TTμL gate driving DTμL Gates.

$$\frac{200}{120} \geq \frac{1 + 1 + \cdots + 1}{10 + 10 + \cdots + 10}$$

Maximum load, 12 DTμL gates, limited by low-level drive capabilities. Here the high-level load equals 12, and the drive capability is 200.

TTμL and LPDTμL devices having active pullups are relatively immune to changes in high-level loads. Their V_{OH} level is primarily set by being 2 V_{BE}'s below Vcc.

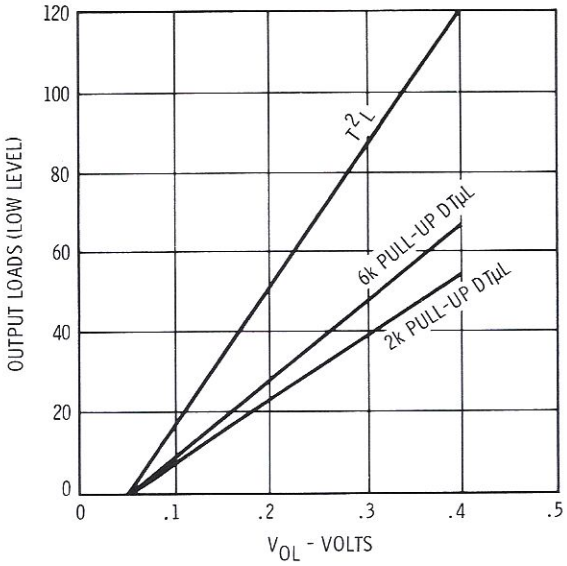


Fig. 3. Gate type elements.

LIMITED LOADING APPLICATIONS

The curves shown in Figs. 3 and 4 show improvements in V_{OL} level for outputs which are not driving the maximum number of loads.

Fig. 3 shows reduction in V_{OL} and hence an improvement in the low-level noise margin for TTμL and DTμL with 6-K or 2-K pullup resistors. Example: A TTμL Gate can drive a maximum of 120 low-level loads and meet a guaranteed V_{OL} of 0.40 volt. If, however, this same output is only driving 50 low-level loads, the worst-case voltage, V_{OL}, at that output would be 0.20 volts and the worst case low level noise immunity would be 0.50 volts.

Fig. 4 shows similar low-level curves for the TTμL and DTμL buffers.

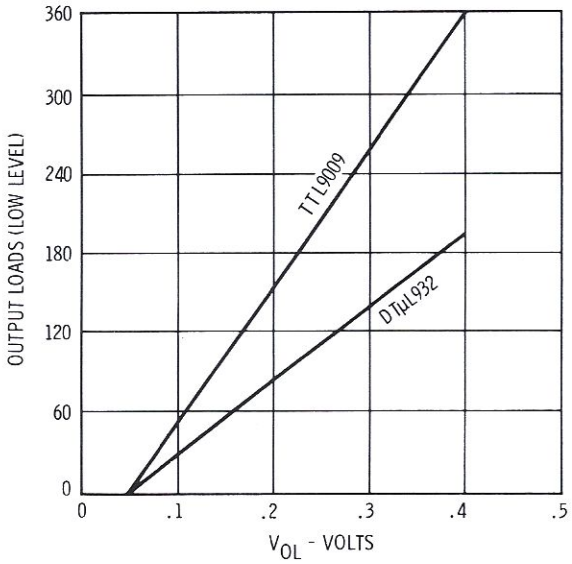


Fig. 4. Buffer elements.

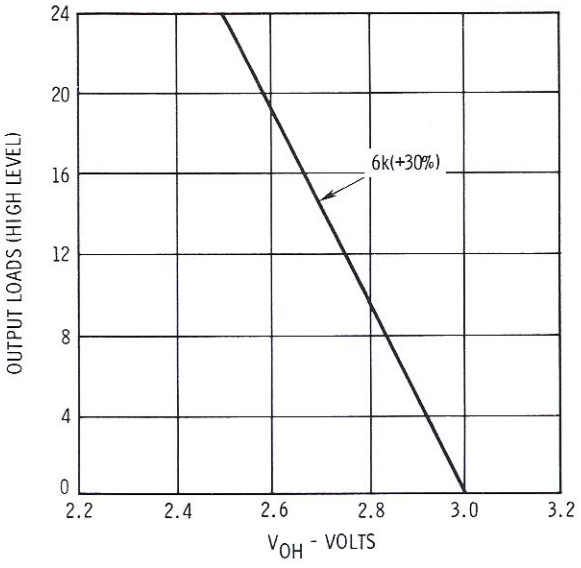


Fig. 5. 6-K pullup.

Fig. 5 shows the increase of V_{OH} of a DTμL output high level if the high-level loads are less than the maximum specified in the CCSL loading rules. This curve is determined by using the +30 percent tolerance resistor and is guaranteed by dc testing.

Fig. 6 shows changes in V_{OH} for DTμL devices which have a 2-K pullup resistor. The test point guarantees a V_{OH} = 4.0 volts with 24 high-level loads being driven. The increased number of loads which can be driven and still meet the CCSL V_{OH} of 2.5 volts is based on worst case maximum tolerance pullup resistor as determined by dc testing. If less than 24 high-level loads are driven, the increase in V_{OH} is determined by the worst case minimum tolerance pullup resistor.

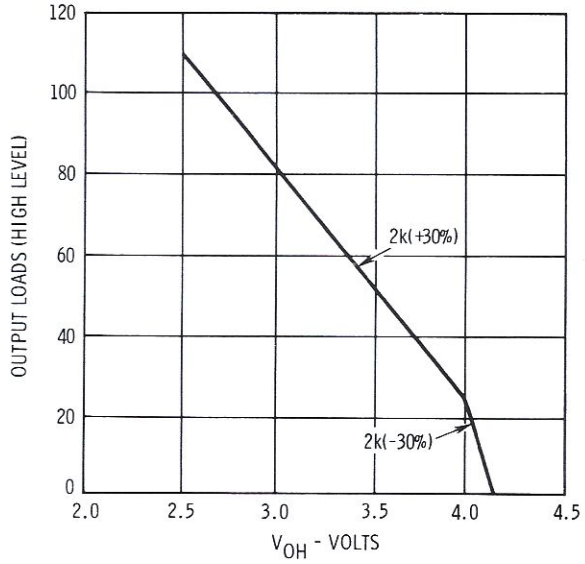
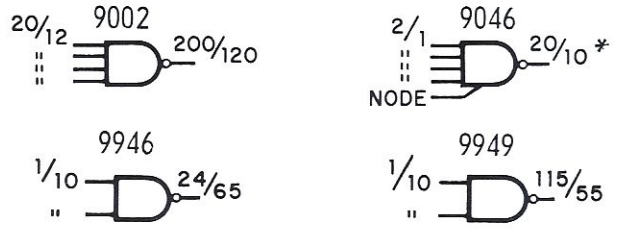


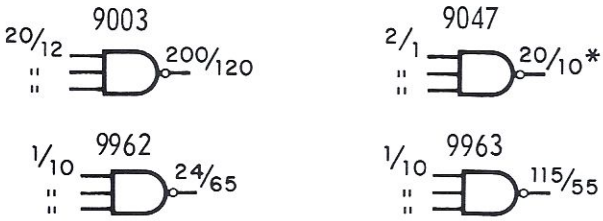
Fig. 6. 2-K pullup.

QUAD 2-INPUT NAND GATES

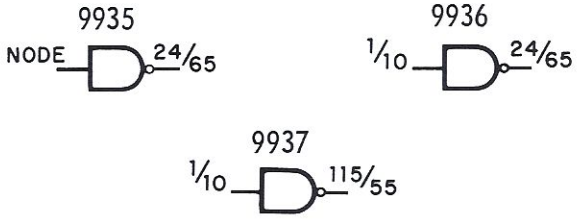


DUAL 4-INPUT EXPANDERS

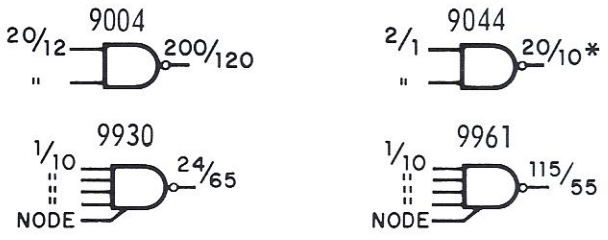
TRIPLE 3-INPUT NAND GATES



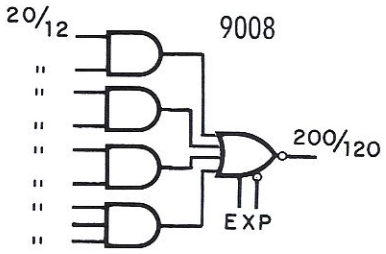
HEX INVERTERS



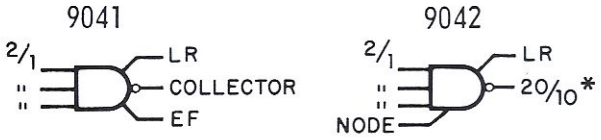
DUAL 4-INPUT NAND GATES



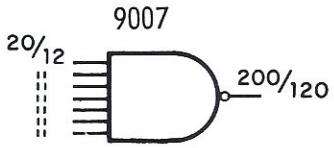
2-2-2-3-INPUT AND/NOR FUNCTION



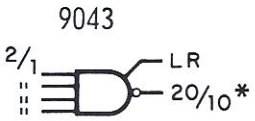
DUAL 3-INPUT NAND GATES



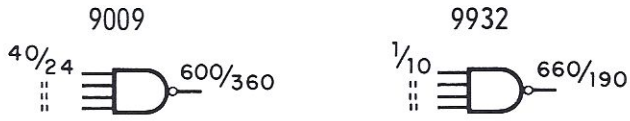
EIGHT-INPUT NAND GATE



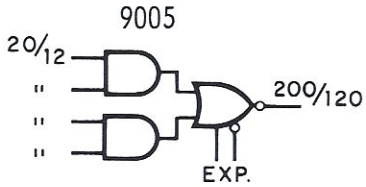
3&4-INPUTS NAND GATES



DUAL 4-INPUT BUFFERS



DUAL AND/NOR FUNCTION



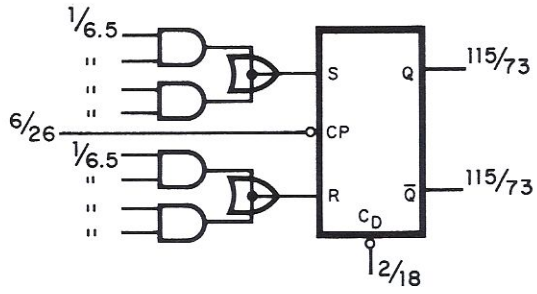
DUAL 4-INPUT DRIVER

* If the minimum temperature is limited to -30°C, the low-level drive factor is 12.

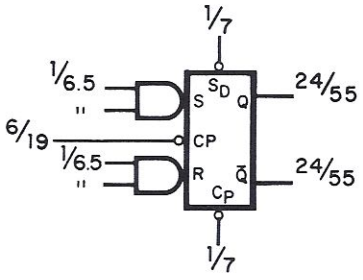
Fig. 7. CCSL input load and drive factors (cont.).

R-S FLIP-FLOPS

9111



9931



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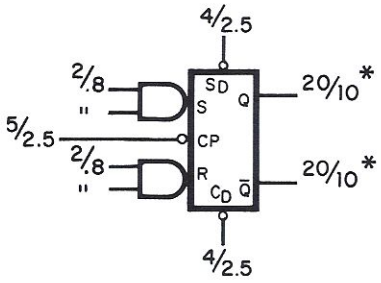

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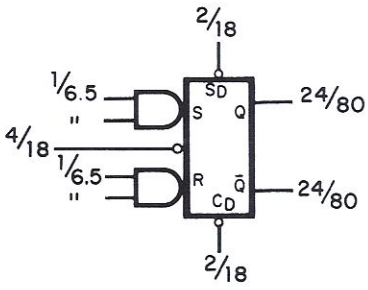

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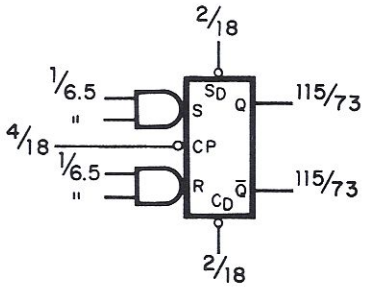
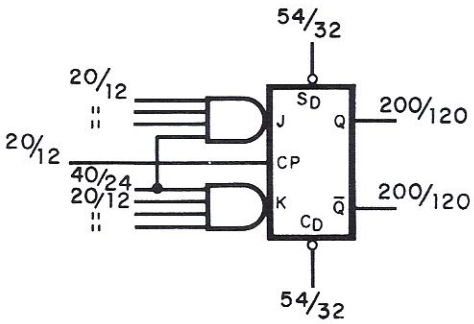


J-K FLIP-FLOPS

9000



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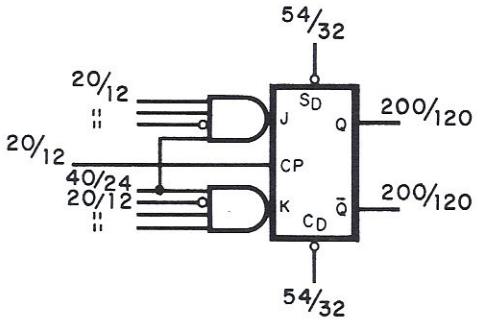
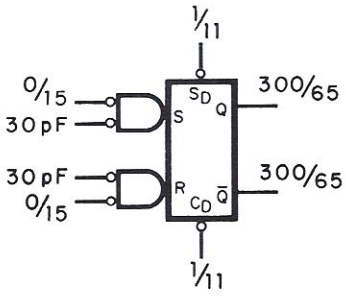


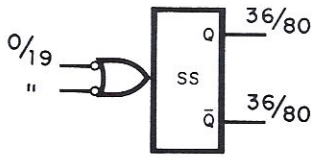
BINARY

9950



ONE-SHOTS (MONOSTABLE)

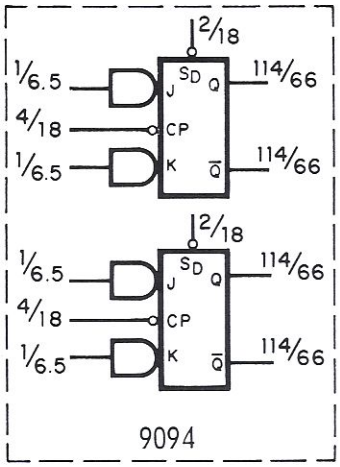
9941 & 9951

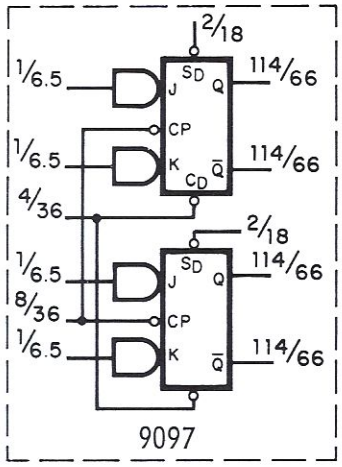


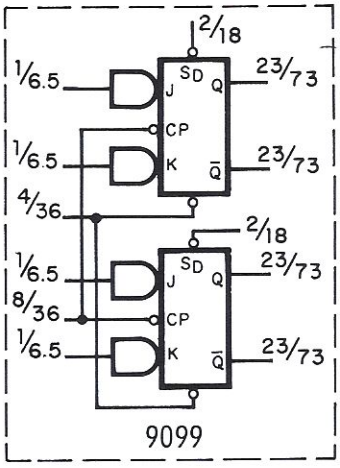
* If the minimum temperature is limited to -30°C, the low-level drive factor is 12.

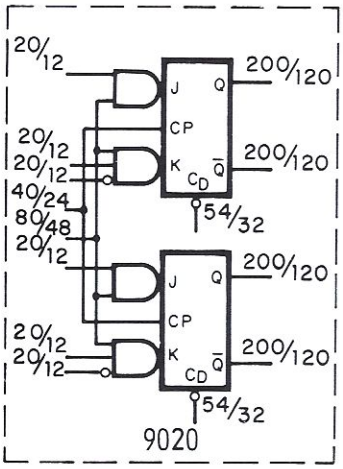
Fig. 7. CCSL input load and drive factors.

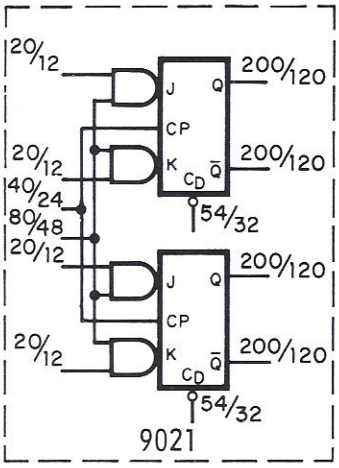
DUAL FLIP FLOPS

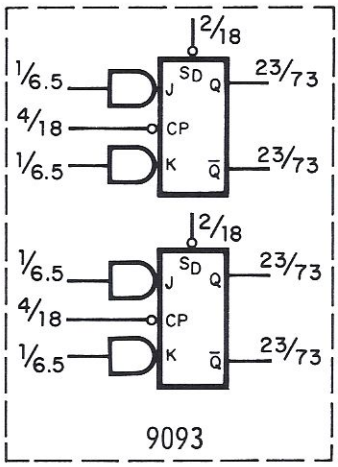


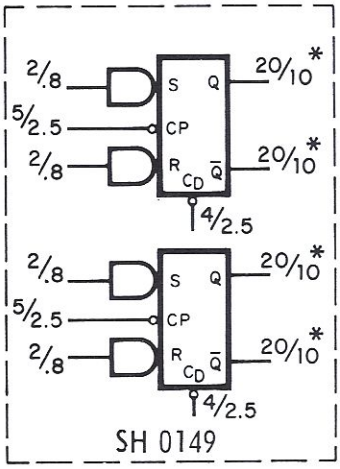


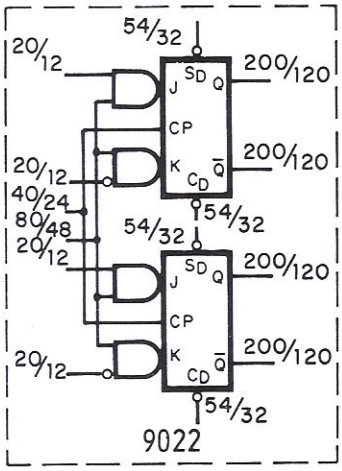


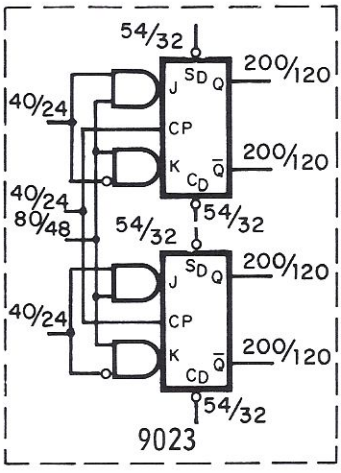












* If the minimum temperature is limited to -30°C, the low-level drive factor is 12.

Fig. 7. CCSL input load and drive factors (cont.).

SPECIAL APPLICATIONS

When using the DTμL 9944 element, the following currents represent unit loads, and must be considered when choosing different collector resistors.

V_{CC}	Load	Temperature (°C)		
		-55	+25	+125
4.5V	High Level	3μA	3μA	5μA
	Low Level	0.121mA	Not worst case	Not worst case
5.5V	High Level	Not worst case	Not worst case	Not worst case
	Low Level	0.151mA	0.154mA	0.146mA

"WIRED OR" APPLICATION

For elements 9930, 9962, 9946, 9935, and 9936, add 24 to the high-level drive factor and subtract 9 from low-level drive factor for each added gate.

For elements 9041, 9043, 9046, and 9048, the high-level drive factor becomes 14 and the low-level drive factor becomes 7. Subtract 2 from the high-level drive factor for each added gate.

APPLICATIONS

This section provides a few applications illustrating the advantage of using the entire CCSL family: DTμL, TTμL and LPDTμL. With CCSL, no irrevocable decision specifying one particular family needs to be made, based on immediate requirements. The balanced capabilities of the various logic types allow a designer to optimize logic capability, speed, and power. CCSL loading rules allow critical speed areas of existing DTμL or LPDTμL systems to be upgraded without changing those portions where speed is less critical.

Choosing the proper speed for the job is important. TTμL with its fast transitions is ideal for high-speed work, but DTμL will perform the same function for low- and medium-speed applications without requiring as many precautions regarding clock skew, power distribution, and long signal lines.

Beyond such differences in speed, the three logic families have many unique logic characteristics which may be used to simplify a design.

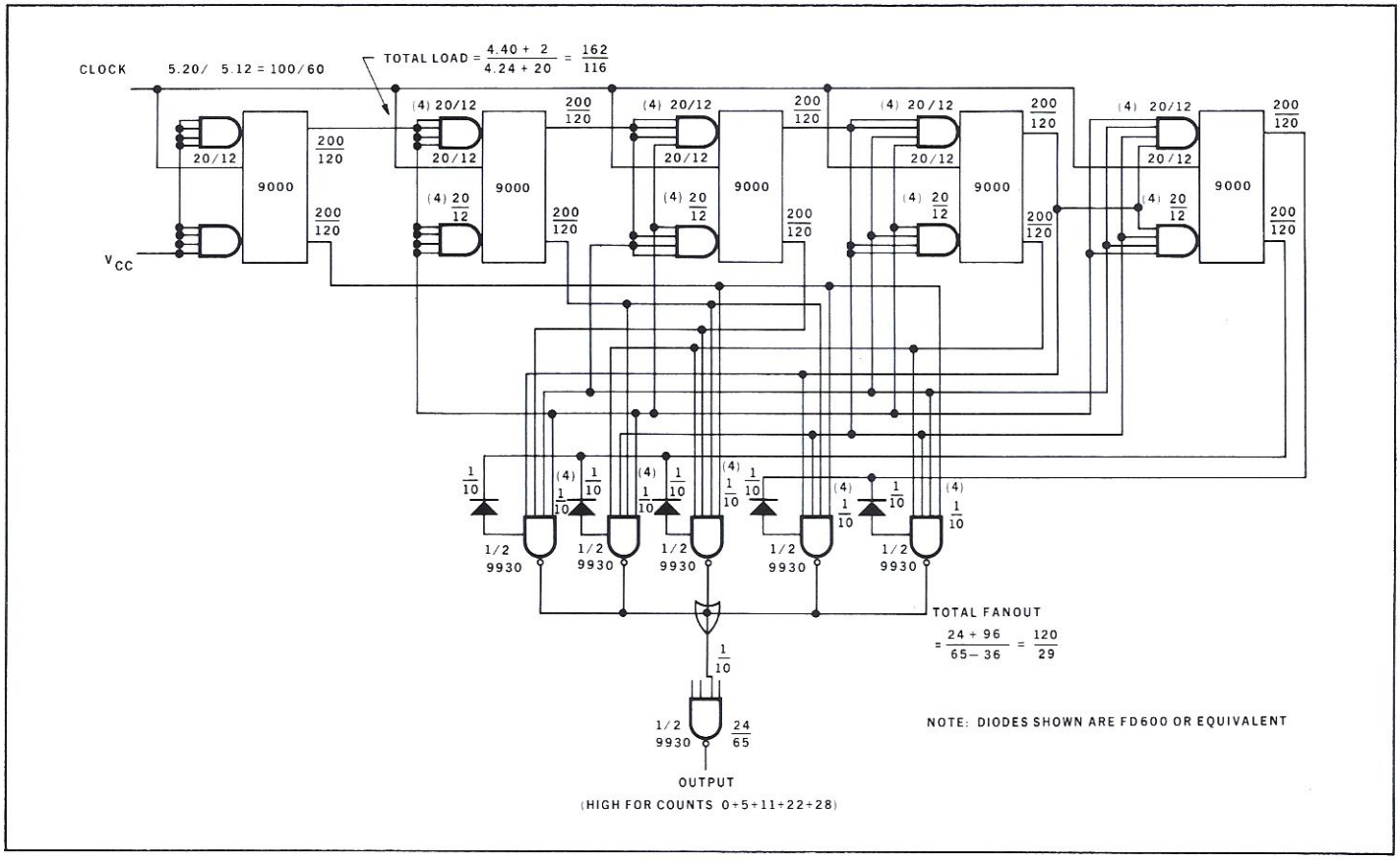


Fig. 8. Five-bit synchronous counter with decoded outputs.

Five-Bit Synchronous Counter

The 5-bit synchronous binary counter with decoded output as in Fig. 8 illustrates some advantages of mixing families. Because the TTμL 9000 flip-flop provides three J, three K, and a JK input, a 5-bit synchronous binary counter may be implemented without additional gating. The TTμL flip-flops have fast propagation delays. When decoded with DTμL gates, no transitory false outputs or "spiking" occurs. A 5-bit binary counter may represent, in binary form, states 0 through 34. The illustrated decoding provides a logic 1 output at states 0, 5, 11, 22, and 28; logic 0 at other states. Five input gates are required; 9930 DTμL NAND gates with their expansion flexibility were chosen. Discrete diodes are shown for the fifth gate input. Almost any switching diode, such as a FD600 may be used.

Shift Register With Multi-Source Parallel Load

The shift register of Fig. 9 illustrates another DTμL-TTμL combination. A shift register is loaded in parallel from one of the multiple sources and shifted out serially at 10 MHz. For a shift register n-bits long, the parallel loading rate is 10/N MHz, allowing DTμL input gating to be used with the "WIRED-OR" simplification. TTμL flip-flops and gates are used for the 10-MHz portion only.

Existing DTμL systems may be upgraded in speed by the selective use of TTμL elements. The replacement is aided by the package pin compatibility of DTμL and TTμL gates.

Binary Full Adder

Fig. 10 illustrates a binary full adder implemented with DTμL 9946 NAND gates. The speed-limiting factor of a parallel adder is carry propagation. Replacement of the two DTμL gates "A" and "B" in the carry generation portion of the adder with pin compatible TTμL 9003 NAND gates reduces a carry propagation delays by a factor of about four.

Where power is at a premium -- such as aerospace, military, or remote-site applications, LPDTμL provides the answer. These compatible medium-speed circuits provide reliable operation over the full -55°C to +125°C military temperature range with power dissipation under 1 mW per gate. Typical gate propagation delays are 60 nsec. A unique output allowing selection of active pullup, resistor pullup, or "WIRED-OR" enhances logic capability.

Low-Power Time-Interval Measurement System

Compatible DTμL or TTμL circuits may be used in combination with the LPDTμL for high-speed, or high-fanout applications. An example of this capability is shown in Fig. 11, a low-power time interval measurement circuit.

External start and stop pulses enable a 40-MHz clock input to a binary counter. The value of the counter at the conclusion of a sample period is a measure of the number 25-ns time increments between the start and stop pulses. A 15-bit counter limits the maximum time interval to 0.82 millisecond. When used in a radar ranging application, this corresponds to a maximum range of 65 miles with a

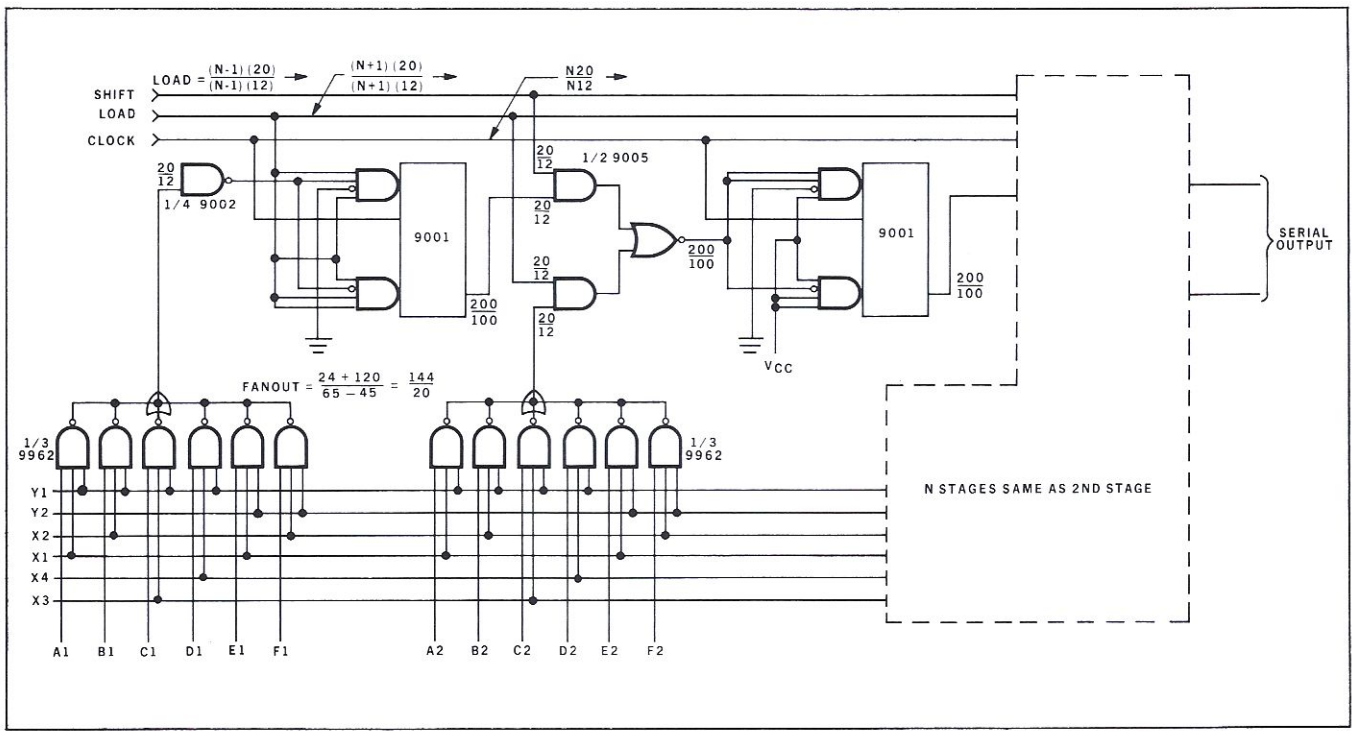


Fig. 9. Shift register with multisource parallel load.

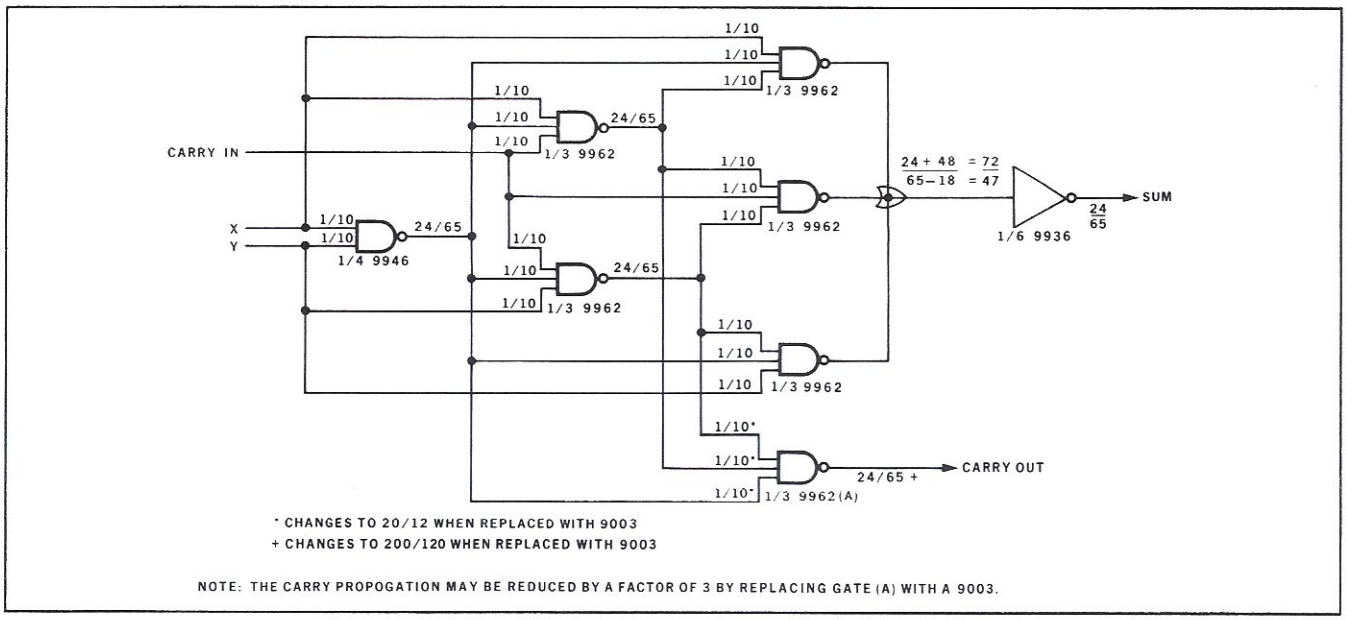


Fig. 10. Binary full adder.

resolution of 12 feet. A TTμL 9001 flip-flop, controlled by 9002 gates is used to provide high-speed switching. Three stages of 9950 DTμL flip-flops count down to 2.5 MHz followed by eleven LPDTμL 9040 stages.

After the stop pulse, the 15-bit time interval number is read out, 5 bits at a time, using LPDTμL 9041 gates. Note the use of the "WIRED-OR" connection. After readout, a TTμL 9002 gate, used as a high-fanout buffer, resets all flip-flops in preparation for another measurement.

Total average power dissipation is 450 mW for this circuit. An all-TTμL implementation would dissipate 2 watts -- over four times that of the CCSL mix.

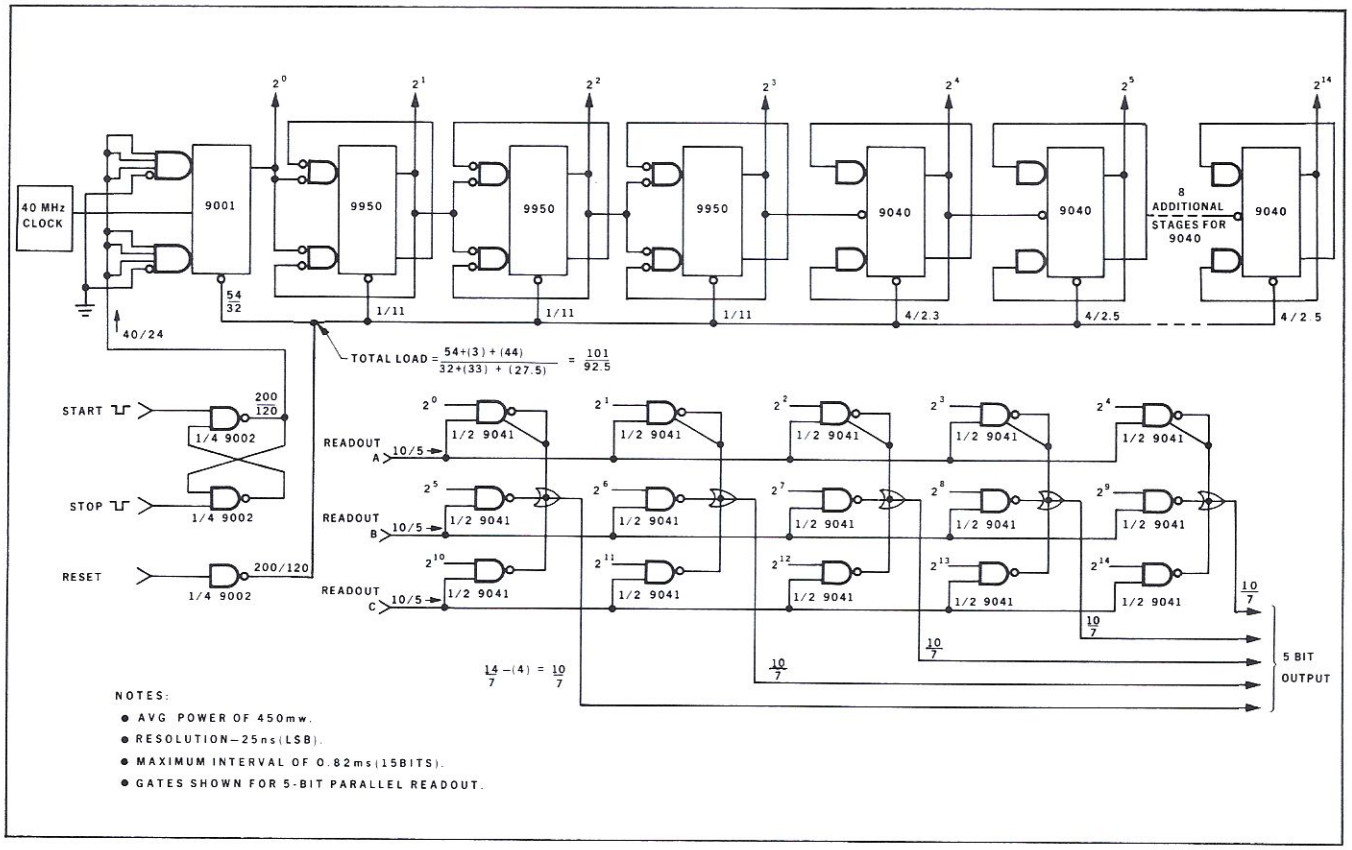
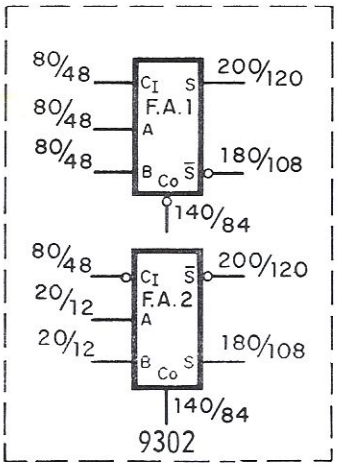
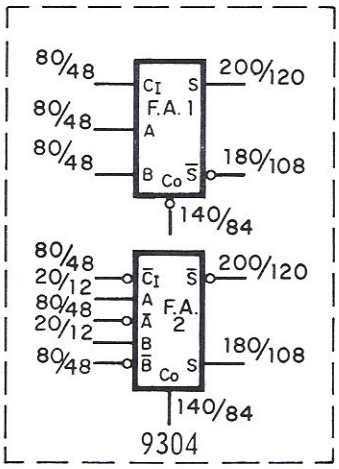


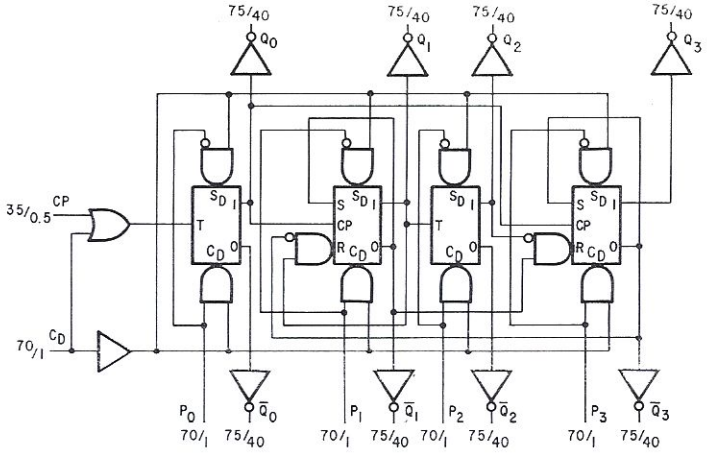
Fig. 11. Low-power time interval measurement system.

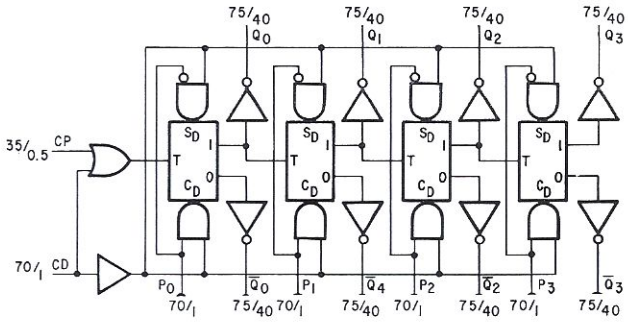
DUAL FULL ADDERS



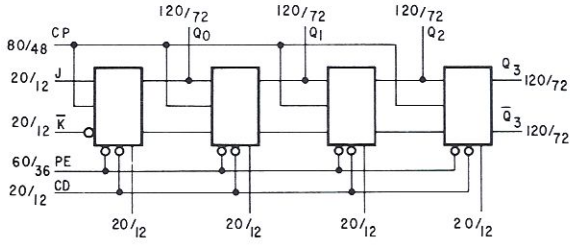


HIGH SPEED COUNTERS





4 BIT SHIFT REGISTERS



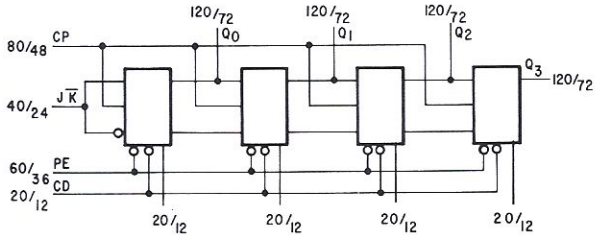


Fig. 12. Complex Functions